Measurements of the PowerPC750 Upset Susceptibility to Protons and Heavy Ions

Gary Swift, Steven Guertin and Farhad Farmanesh
Jet Propulsion Laboratory / California Institute of Technology
Pasadena, California

Short Abstract - Samples of the Motorola PowerPC750, an advanced commercial processor and attractive candidate for space applications, have been irradiated with energetic protons and heavy ions to study resulting single event effects. While no latchups occurred, the registers and caches were soft to upset from both, and a variety of lockups were observed. A simple and powerful test technique, dubbed the "pin wiggler," is highlighted, and the results are compared with those from a more conventional register testing methodology.

For space designs, just as for terrestrial applications, the appetite for more computing power is virtually insatiable. Further, like portable applications, space use implies severe power constraints. Among currently available commercial processors, the PowerPC family ranks high in MIPS per watt, but its suitability for space applications may be limited by the radiation environment, particularly single event effects (SEE). Earlier studies of PowerPC60X processors [1,2] have been encouraging: although soft to upset, the rates may be low enough for some applications. Presented here are new results on the more powerful PowerPC750.

The PowerPC750 contains a number of register types and caches, including general purpose registers (GPRs), floating point registers (FPRs), special purpose registers (SPRs), and L1 instruction and data caches. Upset cross sections per bit have been measured individually for each of these types of storage elements for both one-to-zero and zero-to-one upsets. Additionally, there are several pipelined integer and floating point process units, a memory management unit, a branch prediction table, and the state machines and sequencers to coordinate everything. Upsets in these, as well as certain of the SPRs, can cause a variety of malfunctions that, for purposes of discussion, are called "lockups." Additionally, proton or heavy ion irradiation causes occasional processor exceptions to be invoked. Device cross sections for lockups and exceptions have also been measured, albeit with lower statistics. The existence of features such as dynamic logic storage elements and large trees of combinational logic suggests the likelihood of flux and/or clock rate dependencies. These have not yet been found, although, admittedly, more testing is needed.

Upset testing on the PowerPC750 is made quite difficult by the processor complexity and, particularly, by the ion-induced lockups. "Conventional" register testing requires two main steps: (1) loading registers of interest with known patterns before irradiating and (2) inspecting them for upset bits afterward. Processor complexity and exceptions are handled by suitable complexity in the software executing during irradiation. However, lockups prevent the post-irradiation routines from inspecting for upsets. One method used to circumvent this problem was to perform the inspection using the JTAG port. Of course, sometimes this is impossible because the JTAG functionality has also been upset into lockup. In any case, extracting the

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data required significant (and expensive) time between irradiations when testing with the conventional method.

The "pin wiggler" method of processor upset testing [3] had not previously been tried on a processor of this complexity, but offered potential advantages in data collection efficiency, reduced test preparation and assembly language coding, and clear identification of the occurrence of lockups at the expense of any visibility into their cause. Under this method, a simple self-inspection program is run during irradiation. It uses only three pins to signal processor health, upsets in the registers under inspection, and recoverable and non-recoverable functionality interrupts. The three pins, in this case three unused address lines, are connected to counters that are recorded periodically in a "strip chart" during irradiation. This turned out to be quite successful, and an example strip chart is shown in the figure below.

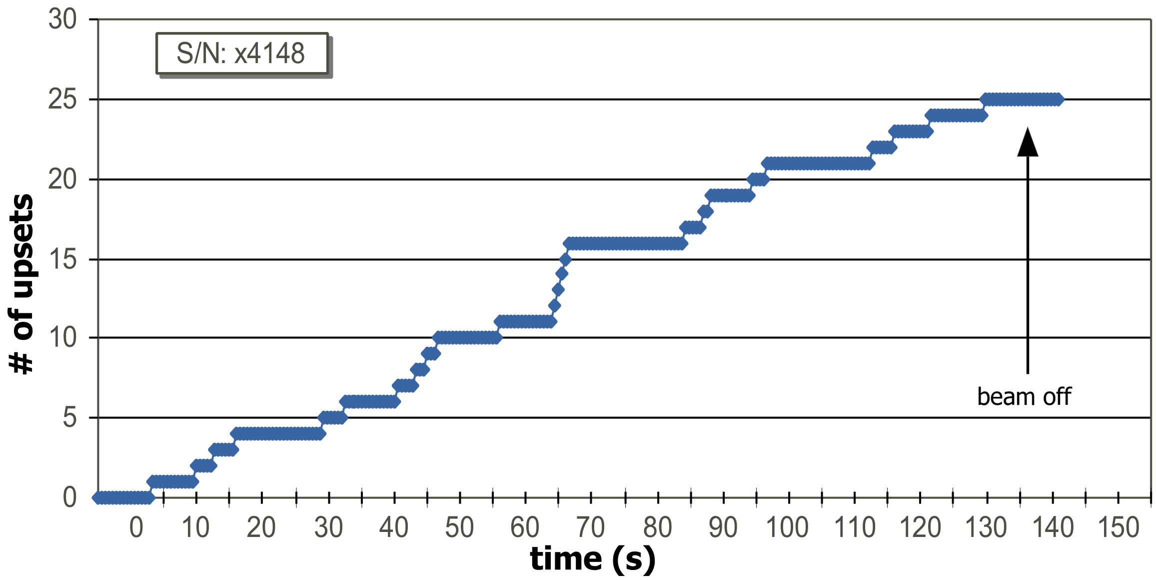

Figure. An example of a pin wiggler strip chart showing the accumulation of 25 zero-to-one upsets in the FPRs (32 registers of 64 bits or 2048 bits) during irradiation with $5 \cdot 10^6$ Ne (140 MeV) ions per cm^2 (LET=4.5 MeV per mg/cm^2). This means the per-bit cross section is $2.4(\pm 0.5) \cdot 10^{-9} \cdot cm^2$ (the one-to-zero cross section is about 5 times bigger). Note that no lockups were observed in this run.

Register testing (from either method) yields results and conclusions similar to those obtained previously for the 60X branch of the PowerPC family: although soft, these processors are usable for some space applications that are not real-time critical. This conclusion is reinforced by the fact that the majority of register upsets (by one or two orders of magnitude) are benign for typical software. Unfortunately, unlike register upsets, the incidence of lockups is expected to increase with more complex software; this needs further investigation. At any rate, error mitigation hardware (like watchdog timers) and software techniques (like redundant code) are desirable and may be required.

[1] F. Bezerra, S. Barde, R. Ecoffet, S. Fourtine, J. Barboule, M.C. Calvet, B. Gagnou, P. Leconte, P. Calvel, D. Hardy, *Commercial Processors Single Event Effect Test,* RADECS Data Workshop, 1997.

[2] P.T. McDonald, W.J. Stapor, and B.G. Henson, *PC603E 32-bit Risc µP Radiation Effects Study,* Innovative Concepts, Inc. White Paper, 1999.

[3] Gary Swift, "A Neat Method for Upset Testing of Microprocessors," presented at the 12th SEE Symposium, Manhattan Beach, Calif., April 2000.